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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/664,746	09/18/2003	Walter G. Fry	200304320-3	4713

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EXAMINER	
PATEL, NIKETA I	

ART UNIT	PAPER NUMBER
2182	

DATE MAILED: 09/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/664,746	FRY ET AL.	
	Examiner	Art Unit	
	Niketa I. Patel	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9,11,14 and 23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,11,14 and 23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/18/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This application is a Continuing Application of application number 09/443,687, field under 37 CFR 1.53(b). The preliminary amendment field on 9/18/2003 is acknowledged.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claim 1 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of U.S. Patent No. 6,636,904 B2. Although the conflicting claims are not identical, they are not patentably distinct from each other because the instant application has a positive recitation of " a first address line and a second address line" whereas the U.S. Patent No. 6,636,904 B has recitation of "a plurality of address line."

4. Claim 11 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 3 of U.S. Patent No. 6,636,904 B2. Although the conflicting claims are not identical, they are not patentably distinct from each other because the instant application has a positive recitation of "a particular system bus address line associated

with a bridge logic device" whereas the U.S. Patent No. 6,636,904 B has recitation of "a particular system bus address line."

5. Claim 23 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of U.S. Patent No. 6,636,904 B2. Although the conflicting claims are not identical, they are not patentably distinct from each other because the instant application has a positive recitation of " a first address line and a second address line" whereas the U.S. Patent No. 6,636,904 B has recitation of "a plurality of address line."

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) The invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-2 are rejected under 35 U.S.C. 102(b) as being anticipated by Staples U.S. Patent Number: 5,799,036 (hereinafter referred to as "*Staples*".)

8. **Referring to claim 1**, *Staples* teaches a computer system, comprising: a processor (see figure 8 – element 102), a system memory (see figure 8 – element 110) coupled to said processor, a bridge logic device coupled to said processor and said system memory and having a peripheral bus interface (see figure 8 – elements 102, 110, 120, 180), wherein said bridge logic device is associated with at least a first address line (see figure 8 – elements 120), a peripheral bus comprising a plurality of address lines, including the first address line, and coupled to the peripheral bus interface of said bridge logic device (see figure 8, bus connection between the

elements 106 and 180 and the bus connection between 180 and 40), said peripheral bus capable of coupling together various peripheral devices (see figure 8 – elements 120, 180, 30, 40, 124, 150); a first peripheral device coupled to said peripheral bus wherein said first peripheral device is associated with said first address line; an input/output device coupled to said bridge logic device', and a logic device coupled to said peripheral bus that swaps a second address line for said first address line when a peripheral bus cycle is run to a said first address line (see figure 8 – element 180, 190)

9. **Referring to claim 2**, wherein said peripheral bus comprises a PCI bus (see figure 8 – element 120.)

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Staples U.S. Patent Number: 5,799,036 (hereinafter referred to as "*Staples*".)

12. **Referring to claim 3**, *Staples* fails to explicitly set forth the limitation of the logic device comprising a PLD. However, *Staples* teaches a host bus adapter which includes a controller logic for selecting different paths through the multiplexer (see column 6 – lines 51-56; column 10 – line 6-36).

It would have been obvious to one of ordinary skill in the art at the time of applicant's invention that a programmable logic device was an old and well-known type of controller logic in the computer art. It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to implement *Staples's* controller logic device as a programmable logic device in order to program control information thereto.

13. Claims 4-9, 11, 14, 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Staples U.S. Patent Number: 5,799,036 (hereinafter referred to as "*Staples*") as applied to claim 1 above, and further in view of Botkin et al. U.S. Patent Number: 6,161,161 (hereinafter referred to as "*Botkin*").

14. **Referring to claim 4**, *Staples* teaches that the logic device swaps the second address line for said first address line when a peripheral bus cycle is run (see column 9 – lines 61-57; column 10 – lines 1-38; column 6 – lines 33-67; column 7 – lines 1-14). *Staples* fails to explicitly fails to explicitly set forth the limitation of a bus configuration cycle. However *Botkin* teaches to perform a bus configuration cycle to select a target device (see *Botkin* column 7 – lines 16-28), permitting an initiator to communicate with the target device.

One of ordinary skill in the art at the time of applicant's invention would have clearly recognized that it is quite advantageous for the peripheral bus cycle of *Staples* to be a bus configuration cycle to allow an appropriate target device to be selected. It is for this reason that one of ordinary skill in the art would have been motivated to substitute *Staples's* peripheral bus cycle with a bus configuration cycle to permit configuration of a target device.

15. **Referring to claim 5**, the system of *Staples* as modified by the system of *Botkin* as applied to claim 4 above teaches that the logic device issues a retry to the bridge logic, which, in response, issues a retry to said processor (see *Botkin* column 6 – lines 42-60).

1. **Referring to claim 6**, the system of *Staples* as modified in claim 3 above and by the system of *Botkin* as applied to claim 4 above teaches wherein said peripheral bus comprises a PCI bus including said first address line and said second address line and said logic device is a programmable logic device that detects a PCI configuration cycle run for one of the address lines comprising the PCI bus (see *Staples* column 9 – lines 61-57; column 10 – lines 1-38; column 6 – lines 33-67; column 7 – lines 1-14; figure 8 – elements 120, 180, 30, 40, 124, 150; and *Botkin* column 7 – lines 16-28.)

16. **Referring to claim 7** the system of *Staples* as modified by the system of *Botkin* as applied to claim 6 above teaches further comprising an electronically controlled switch coupled to and controlled by said programmable logic device, said switch receiving at least two PCI bus address lines (see *Staples* figure 8 – element 190.)

2. **Referring to claim 8**, the system of *Staples* as modified by the system of *Botkin* as applied to claim 6 above teaches wherein said programmable logic device switches the two PCI bus address lines when the programmable logic device detects a PCI bus configuration cycle targeted for one of the two address lines so that the address line targeted by the PCI bus configuration cycle is electrically connected to the other of said two address lines (see *Staples* column 9 – lines 61-57; column 10 – lines 1-38; column 6 – lines 33-67; column 7 – lines 1-14; and *Botkin* column 7 – lines 16-28.)

17. **Referring to claim 9**, the system of *Staples* as modified by the system of *Botkin* as applied to claim 6 above teaches further including a PCI device connected to said PCI bus that has its IDSEL input pin connected to one of said two address lines (see *Botkin* column 7 – 9-28.)

18. Claim 10 is Cancelled.

19. **Referring to claim 11**, (Currently amended) A programmable logic device coupled to a system bus comprising a plurality of address lines, said programmable logic device having logic that detects configuration read or write cycle to a particular system bus address line associated with a bridge logic device and, upon detecting a configuration read or write cycle to that particular address line, the programmable logic device asserts a control signal to an electronically-controlled switch to connect the particular system bus address line to another address line.

20. Claim 12 is Cancelled.

21. Claim 13 is Cancelled.

22. **Referring to claim 14**, (Original) the system of *Staples* as modified by the system of *Botkin* as applied to claim 11 teaches wherein programmable logic device issues a retry signal upon detecting the configuration read or write cycle to the said particular address line (see *Botkin* column 6 – lines 42-60.)

23. Claims 15-22 are Cancelled.

24. **Referring to claims 11 and 23**, *Staples* teaches a system and method comprising: a processor (see figure 8 – element 102), a bridge logic device coupled to said processor and a comprises a plurality of address lines including a first address line (see figure 8 – element 190, 30 124); at least one system bus peripheral device connected to said system bus (see figure 8 –

element 180), wherein said at least one system bus peripheral device is associated with said first address line (see figure 8, bus connection between the elements 106 and 180 and the bus connection between 180 and 40); an electronically-controlled switch connected to at least said first address line (see figure 8 – element 190); and system bus that a means for detecting a system bus configuration cycle associated with a said first address line and, upon detecting the configuration cycle associated with said first address line, asserting a control signal to said switch to connect said first address line to another of the system bus address lines associated with said first peripheral device (see column 9 – lines 61-57; column 10 – lines 1-38; column 6 – lines 33-67; column 7 – lines 1-14.) *Staples* fails to explicitly fails to explicitly set forth the limitation of a bus configuration read or write cycle. However *Botkin* teaches to perform a bus configuration read or write cycle to select a target device (see *Botkin* column 7 – lines 16-28), permitting an initiator to communicate with the target device.

One of ordinary skill in the art at the time of applicant's invention would have clearly recognized that it is quite advantageous for the peripheral bus cycle of *Staples* to be a bus configuration read or write cycle to allow an appropriate target device to be selected. It is for this reason that one of ordinary skill in the art would have been motivated to substitute *Staples's* peripheral bus cycle with a bus configuration read or write cycle to permit configuration of a target device.

Response to Arguments

25. Applicant's arguments filed 09/18/2003 have been fully considered but they are not persuasive. The applicant argues that (1) *Staples* does not teach that the bridge and the first peripheral device are both associated with a first address line and (2) there is mp motivation in the art to suggest combining *Staples* and *Botkin* (at pages 7-9 of the Remarks section). The examiner respectfully disagrees with these arguments.

As per the first argument, *Staples* teaches that the bridge and the first peripheral device are both associated with a first address line (see figure 8, bus connection between the elements 106 and 180 and the bus connection between 180 and 40.)

In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, *Botkin* discloses that in order to select a target device on a PCI bus a PCI configuration cycle needs to be performed.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Niketa I. Patel whose telephone number is (571) 272 4156. The examiner can normally be reached on M-F 8:00 A.M. to 5:00 P.M.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dov Popovici can be reached on (571) 272 4083. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NP
08/30/2005

KIM HUYNH
PRIMARY EXAMINER
9/1/05